

REMARKS

Claims 1-20 remain in the application for consideration of the Examiner.

Reconsideration and withdrawal of the outstanding rejections are respectfully requested in light of the above amendments and following remarks.

Turning now to the art rejection, Claims 1, 2, 7, 10, 16, and 19 were rejected under 35 U.S.C. § 102(b) as being anticipated by Sauer; Claims 3, 4, 6, 8, 9, 12, 13, 15, 17, 18, and 20 were rejected under 35 U.S.C. § 103 as being unpatentable over Sauer.

These rejections are respectfully traversed.

It is respectfully submitted that Sauer does not disclose or suggest the presently claimed invention including the first circuit operable with the first supply rail and a second circuit operable with the second supply rail as defined in independent Claims 1 and 10, albeit defined as the first transistor circuit operable with the first supply rail and the second transistor circuit operable with the second supply rail in independent Claim 19.

Sauer fails to disclose this aspect.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant response places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, Applicant petitions for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,



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TI-35630 Page 8